WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a gate oxide located over a substrate; and

a silicided gate electrode located over said gate oxide, said silicided gate electrode including a first metal and a second metal.

2. The semiconductor device as recited in Claim 1 further including a dopant located within and configured to tune a work function of said silicided gate electrode.

3. The semiconductor device as recited in Claim 2 wherein said dopant is selected from a group consisting of:

boron;

phosphorous; and

arsenic.

4. The semiconductor device as recited in Claim 1 further including source/drain regions located in said substrate proximate said gate oxide and silicided source/drain contact regions located in said source/drain regions, wherein said silicided source/drain contact regions have a depth substantially different than a thickness of said silicided gate electrode.

5. The semiconductor device as recited in Claim 4 wherein said silicided gate electrode is silicided with a different metal than said silicided source/drain contact regions.

6. The semiconductor device as recited in Claim 1 wherein said first metal is cobalt and said second metal is nickel.

7. The semiconductor device as recited in Claim 6 wherein a ratio of an atomic percent of said cobalt to said nickel in said silicided gate electrode ranges from about 9:1 to about 2:3.

8. The semiconductor device as recited in Claim 7 wherein said atomic percent ranges from about 3:1 to about 1:1.

9. The semiconductor device as recited in Claim 1 wherein said silicided gate electrode has a thickness ranging from about 15 nm to about 150 nm.

10. A method for manufacturing a semiconductor device, comprising:

placing a gate oxide over a substrate; and

forming a silicided gate electrode over said gate oxide, said

silicided gate electrode including a first metal and a second metal.

11. The method as recited in Claim 10 wherein said forming includes depositing a blanket layer of polysilicon material over a blanket layer of gate oxide material, depositing a blanket layer of a cobalt-nickel bilayer or a blanket layer of cobalt-nickel alloy over said blanket layer of polysilicon material, and annealing said layers to form a blanket layer of silicided gate electrode material including cobalt and nickel.

12. The method as recited in Claim 11 further including patterning said blanket layer of silicided gate electrode material to form said silicided gate electrode including cobalt and nickel.

13. The method as recited in Claim 11 further including implanting a dopant into said blanket layer of polysilicon material to tune a work function of said silicided gate electrode.

14. The method as recited in Claim 13 further including forming a capping layer over said cobalt-nickel bilayer or cobalt-nickel alloy, said capping layer configured to affect a doping profile of said dopant.

15. The method as recited in Claim 14 wherein said capping layer comprises a transition metal-nitride.

16. The method as recited in Claim 11 wherein a ratio of a thickness of said cobalt layer to a thickness of said nickel layer ranges from about 9:1 to about 2:3.

17. The method as recited in Claim 11 wherein said cobalt - nickel alloy has a Co_x to Ni_y ratio (x:y) ranging from about 9:1 to about 2:3.

18. The method as recited in Claim 11 wherein a ratio of an atomic percent of said cobalt to said nickel in said silicided gate electrode ranges from about 9:1 to about 2:3.

19. The method as recited in Claim 10 further including forming source/drain regions in said substrate and forming silicided source/drain contact regions in said source/drain regions subsequent to forming said silicided gate electrode.

20. An integrated circuit, comprising:

transistors located over a substrate, said transistors including;

a gate oxide located over said substrate;

a silicided gate electrode located over said gate oxide, said silicided gate electrode including a first metal and a second metal; and

an interlevel dielectric layer located over said substrate, said interlevel dielectric layer having interconnects located therein for contacting said transistors.